TRANSLATION FROM GERMAN

(12) International application published pursuant to the Treaty on International Patent Cooperation (PCT)

(19) World Organization for Intellectual Property International Office

(43) International Publication Date: October 25, 2001
(10) International Publication Number: **WO 01/80322 A2**
(51) International Patent Classification': H01L 33/00

(21) International File Number: PCT/EP01/01513
(22) International Filing Date: April 19, 2001

(25) Filing language: German
(26) Publication language: German

(30) Priority Data: 100 19 666.9 April 19, 2000 GE

(71) Applicant (for all treaty state except the US) OSRAM SEMICONDUCTORS GMBH & CO, OHG [GE/GE]; Wernerwerkstrasse 2, 93049 Regensburg (GE).

(72) Inventor and
(75) Inventor/Applicant: (only for US): BOGNER, Georg [GE/GE]; Am Sandbuegel 12, 93138 Lappersdorf (GE). KUGLER, Siegmar [GE/GE]; Coulmiersstrasse 1, 93055 Regenburg (GE). NEUMANN, Gerald [GE/GE]; Augustenstrasse 19, 93049 Regensburg (GE). NIRSCHL, Ernst [GE/GE]; Roither Weg 7a, 93173 Wenzenbach (GE). OBERSCHMID, Raimund [GE/GE], Minoritenweg 7 B, 93161 Sinzing (GE). SCHLERETH, Karl-Heinz [GE/GE], Akazienweg 21, 93133 Burglengenfeld (GE). SCHOENFELD, Olaf [GE/GE]; Kollwitz-Strasse 55, 93055 Regensburg (GE); STATH, Norbert [GE/GE]; Rosinusweg 11, 93049 Regensburg (GE)

(74) Attorney: EPPING HERMANN & FISCHER, PO Box 12 10 26, 80034 Munich (GE)

(81) Treaty states (national): CA, CN, JP, KR, US

(84) Treaty states (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR)

(54) **High-Radiance LED Chip and a Method for Producing Same**

(57) **Abstract:** The invention relates to a high-radiance LED chip (1) comprising a radiation-emitting active region (32) and a window layer (2). In order to increase the radiant yield, the cross-sectional surface of the radiation-emitting active region (32) is smaller than the cross-sectional surface of the window layer (2), which is made available for disengaging the light. The invention also relates to a method for producing a lens structure on the surface of a light emitting component.

Published

- *Without international search report and to be re-published after receipt of report*

Refer to the Explanations ("Guidance Notes on Codes and Abbreviations") at the beginning of each regular edition of the PCT Gazette for an explanation of the two-letter codes and other abbreviations.

Specification

LED chip and process for its manufacture

The invention relates to a LED [light emitting diode] chip as claimed in the preamble of claim 1 and a process for producing it.

Semiconductor materials for LED chips in part have a refractive index of far above 3. The medium which borders the chip in conventional LED components, usually air or plastic, has a much lower refractive index. The significant, sudden change which is associated with it in the refractive index on the

interface between the LED chip and the bordering medium leads to a comparatively small boundary angle of total reflection so that most of the electromagnetic radiation which is produced in the active area of the chip is reflected back from this interface into the chip.

For this reason, only a very small portion of the radiation which is produced in the active zone is decoupled directly out of the chip. In conventional LED chips a decoupling portion of only a few percent is computed per flat decoupling surface.

US 5,233,204 proposes, for improving the light decoupling from LED chips, a thick transparent layer which is applied epitaxially in addition to the light-producing layers and which is designed to increase the light decoupling portion through the front of the chip.

Furthermore, the use of highly refractive transparent casting compounds is known, but they have not become popular for cost reasons, among others. In addition, the best casting compounds available to date have a refractive index of at most n=1.6; this results in an overly dramatic, sudden change on the decoupling surface of the light-emitting semiconductor component and thus high reflection losses. Furthermore, the highly transparent casting compounds have undesirable chemical and mechanical properties; this likewise limits large-scale technical use.

The object of the invention is to make available a LED chip in which the ratio of generated to decoupled radiation is improved compared to conventional chips, and which can be installed in conventional LED housing designs. At the same time a process for its manufacture will be devised which compared to conventional methods for producing LED chips requires only little additional technical complexity.

This object is achieved by a LED chip with the features of claim 1 and by a process with the features of claim 22.

Advantageous developments of the LED chip and of the process are the subject matter of dependent claims 2 to 21 and 23 to 25.

With the invention, the radiation yield in a LED chip is increased by narrowing the light-emitting region to an area which is smaller than the cross sectional area of the LED chip. Compared to the usual execution of the light-emitting surface over the entire cross section of the LED chip an increase of decoupling by more than 30% is even possible.

As claimed in the invention there is a LED chip with a radiation-emitting active area with a lateral cross sectional

area F_L and a radiation-transparent window layer downstream of the radiation-emitting active area in the emission direction, with a refractive index n_s which has a lateral cross sectional area F_c for light decoupling and which has a decoupling surface which borders a medium with a refractive index n_M, the cross sectional area F_L of the radiation-emitting active area being smaller than the cross sectional area F_c of the decoupling surface so that the relation

$$F_L \leq \left(n_M / n_S\right)^2 \cdot F_C$$

is satisfied. The cross sectional area F_c relates to the regions of the window layer which are intended for light decoupling or which are available for light decoupling. Here a window layer is defined as both an individual layer and also a multilayer structure which overall performs the function of a window layer.

According to one especially preferred embodiment of the invention, it is provided that the light emission limitation means is made such that the current flow within the LED chip, especially into and/or through the active layer, is limited to the light-emitting area. In this way the emission of light as claimed in the invention can be limited especially easily to a smaller region.

In one embodiment of the invention it is provided that for the thickness H of the window layer the following applies:

$$H < \left(n_S / n_M\right) \cdot \frac{1}{2} \cdot C$$

C being the lateral cross sectional length of the window layer or the effective reflex surface, n_s being the refractive index of the material of the active layer or the window layer and n_M being the refractive index of the material bordering the window layer. The advantage which has been achieved hereby is a further increase of the decoupled amount of light.

Here and below the lateral cross sectional length is defined as the characteristic extension of the corresponding cross sectional area. For a square surface for example this is the length of one side, for a circular surface the diameter. In a different surface shape the lateral cross sectional length can be a value which lies between the maximum and minimum diameter which runs through the center of mass of the surface.

Preferably the following applies to the thickness H of the window layer bordering the active layer.

$$H = (C - D) \cdot \left(2 \cdot \left(n_S / n_M\right)\right)^{-1}$$

C being the lateral cross sectional length of the window layer, D being the lateral cross sectional length of the light-emitting region of the active layer, n_S being the refractive index of the window layer to be transilluminated and n_M being the refractive index of the material bordering the window layer. Up to this level total reflection on the lateral surfaces of the window layer is largely avoided so that decoupling of the generated radiation through the lateral surfaces is possible.

According to another preferred embodiment of the invention the light-emitting region consists of several component luminous regions (33 to 35) of the active layer (3) which are located at a regular interval to one another, the following applying to the entire area F_L of the component luminous areas:

$$\sum_i F_{Li} = F_L \leq \left(n_M / n_S\right) \cdot F_C$$

F_C being the cross sectional area or the basic area of the window layer and thus the effective reflex surface, F_{Li} being the areas of the individual component luminous areas, n_S being the refractive index of the active layer or the window layer and n_M being the refractive index of the material bordering the window layer. In this way light decoupling from the LED chip is optimized in a likewise advantageous manner, as in a central light-emitting region. Accordingly the following applies to the thickness H of the window layer:

$$H = p \cdot A$$

A being the regular interval of the individual component luminous areas and p being a factor which can be chosen between 0.5 and 5.

Advantageously there is an optical means which concentrates the light emerging from the LED chip and which is made on the surface of the window layer. In this way the shape of the emerging light beam can be determined and decoupling can be further increased by suitable choice of material and shape.

One preferred embodiment of the invention calls for the optical means to be formed by one or more, preferably spherical lens(es) with a center point which lies over the center of mass

of the light-emitting region or over the center of mass of the individual component luminous areas.

One likewise preferred embodiment of the invention calls for the optical means to be made by one or more Fresnel lens(es) with a center point lying over the center of mass of the light-emitting region or over the center of mass of the individual component luminous areas.

Preferably the optical means is placed or molded on the surface of the window layer or is formed or shaped out of the window layer.

In another embodiment of the invention the light emission limitation means is formed by a limitation of the active layer, the luminous capacity of the active layer being limited to the light-emitting region.

One advantageous embodiment of the invention is that the light emission limitation means is formed by an insulation layer which consists of a material which is of limited translucency and/or which is at least partially opaque to the emission light of the active layer and which is formed on or at the active layer. In this way the active layer, as was conventional in the past, can run as a continuous layer in a wafer which still contains several individual light-emitting semiconductor components.

Another advantageous embodiment of the invention calls for the light emission limitation means to be formed by an insulation layer which is made on or at the active layer and between the active layer and the power supply and which minimizes the power supply and current flow to or through the active layer in regions outside of the light-emitting region. Here the active layer can also run as a continuous layer in a wafer which still contains several individual light-emitting semiconductor components.

Advantageously the insulating layer consists of a nonconductive oxide layer which is applied on the side of the window layer opposite the effective reflex surface. In this way the power supply can be masked in an especially simple and economical manner. Advantageously the oxide layer is produced by oxidation of the already existing material.

Likewise, the light emission limitation means is advantageously formed by the configuration of the power supply such that the power supply is in electrically conductive contact with the active layer only in contact areas.

According to one preferred embodiment of the invention a second power supply is formed by the electrical contact which

does not completely cover it on the effective reflex surface or on the optical. Conventionally a bond wire for making contact can be attached to it.

A second power supply is likewise advantageously formed by an electrical contact which is connected to the window layer between the active layer and the effective reflex surface.

In another embodiment of the invention a second power supply is formed by an electrical contact connected to the active layer.

Advantageously the power supplies and/or the insulating layer are reflective for the emitted light. In this way the radiant efficiency is further increased by preventing losses.

Advantageously the reflection means for the emitted light is formed on the side of the active layer which faces away from the effective reflex surface in or on the window layer or the active layer. This in turn increases the radiant efficiency further by preventing losses. Accordingly the reflection means is a Bragg grating.

In another embodiment of the invention the window layer and/or the optical means is at least partially provided with a jacket which is transparent to the emission light. In this way the light-emitting semiconductor component is protected against ambient effects. An external shape which corresponds to many applications is thus enabled.

The process as claimed in the invention for producing a lens structure on the surface of the LED chip calls for the lens structure to be shaped on the outside surface of the light-emitting component intended for light exit and passage by means of a cutting tool or etching process from the light-emitting component into the outside surface.

Another preferred process step calls for a spherical lens or a Fresnel lens to be produced as the lens structure.

One especially advantageous process step calls for the lens structure to be produced simultaneously with separation by means of a suitably shaped device for separating the light-emitting components still in the wafer array when they are separated.

Other advantages, particulars and feasible developments of the invention follow from the dependent claims.

The invention is explained below using the drawings. In particular

Figure 1 shows a schematic cross section of one preferred

embodiment of the light-emitting semiconductor diode as claimed in the invention with a light-emitting area of the active layer;

Figure 1a shows a schematic cross section of the embodiment from Figure 1, looking in direction X;

Figure 2 shows a schematic cross section of another preferred embodiment of the light-emitting semiconductor diode as claimed in the invention with a Fresnel lens structure;

Figure 3 shows a schematic cross section of another preferred embodiment of the light-emitting semiconductor diode as claimed in the invention with a Fresnel lens structure;

Figure 4 shows a schematic cross section of another preferred embodiment of the light-emitting semiconductor diode as claimed in the invention with several emitting component luminous areas and a multiple lens structure; and

Figure 5 shows a schematic cross section through a wafer with light-emitting semiconductor components which are still to be separated and which have already been separated and a saw blade which is used for this purpose.

In the following Figures 1 to 5 the same reference numbers label the same or identically working components.

Figure 1 shows a LED chip 1 as claimed in the invention in cross section. The semiconductor component here is composed of a window layer 2 which is radiation-transparent to the emission light, an active layer 3 which emits the light, an optical means for shaping the exit light beam in the form of a lens 41, an insulating layer 5 as the light emission limitation means and a first power supply 71 and a second power supply 6. The window layer 2 is used here moreover as the substrate of the LED chip 1.

The light-emitting region 32 of the active layer 3 is limited in its size and shape and defined by the masking of the insulating layer 5. The shape of the electrical insulation enables contact of the power supply 6 which is formed flat on the bottom of the light-emitting semiconductor component 1 opposite the effective reflex surface at the locations with the chip or with the active layer, above which the light-emitting region 32 is located. In the example an oxide layer is used as the material of the insulation layer. The power supply 6 can be formed by a metal which has been applied flat over the insulating layer 5. No current flows through the regions 31 of the active layer 3 which are not intended for emission, by which light emission does not take place in these regions. The second power supply takes place by the first power supply 71 which is made on the electrically conductive lens 41 in the form of an electrical

contact ("pad") and on which a bond wire can be attached in the conventional manner.

The emission light from the light-emitting region 32 of the active layer 3 with a total area F_L which meets the aforementioned condition

$$F_L \leq \left(n_M / n_S\right)^2 \cdot F_C$$

penetrates through the window layer 2 with the refractive index n_S and thickness H, the following applying;

$$H = (C - D) \cdot \left(2 \cdot \left(n_S / n_M\right)\right)^{-1}$$

The emission light is coupled into the lens body 41 on the effective reflex surface 8 and the exit light beam is formed according to the shape of the lens.

For the thickness of the window layer, for example for a chip with a side length C = 300 microns with $n_S/n_M = 3.5$ in the optimum case D = 100 microns and H = 30 microns. Or according to the following condition

$$H < \left(n_S / n_M\right) \cdot \frac{1}{2} \cdot C$$

H = 500 microns; this represents the maximum allowed value.

Here advantageously the refractive index of the window layer 2 and of the material of the lens body 41 is as similar a possible in order to prevent the aforementioned reflection losses. The optical means is best produced from the window layer 2 itself.

Figure 1a shows the light-emitting semiconductor component 1 from Figure 1, looking in direction X. The active layer 3 here occupies the entire cross sectional area F_C (in the mathematical example from above, 90000 square microns) of the semiconductor component. The light-emitting region 32 has a total area of F_L (in the mathematical example from above 10000 square microns).

Figure 2 shows the cross section of a light-emitting semiconductor component 1 as claimed in the invention which has been soldered on a board 10, here the power supplies 6 and 72 both being mounted on the bottom of the semiconductor component 1. This enables easier soldering of the light-emitting component 1 to the solder surfaces 101 and 102 which are made on the board

10 by means of solder 9. This enables light sources in a so-called SMD design, the light-emitting semiconductor component 1 being hardly larger than a chip itself. In turn, the active layer 3 is made flat and the light-emitting region 32 is defined by an insulating layer 5 as the light emission limitation means. Instead of a lens as in Figure 1, here the optical means for changing the exit light beam is a so-called Fresnel lens 42 which is made on the effective reflex surface of the window layer 2 by means of the process as claimed in the invention by rapidly rotating cutting tools or suitable etching techniques over the light-emitting area 32.

Figure 3 shows another soldered LED chip 1 in cross section, by means of a power supply 73 current feed taking place within the active layer 3. The optical means is a Fresnel lens 43 which was stamped on subsequently.

Figure 4 shows another cross section through a LED chip 1, there being several light-emitting regions 33 and 35 with a total area of the individual surfaces F_{Li} representing the total area F_L of the light-emitting region which in turn meets the aforementioned condition for the ratio of F_L to the basic area F_C of the chip and thus the area of the effective reflex surface.

The height H of the window layer to be transilluminated here should be chosen to be 0.5 to 5 times the distance A of the individual component luminous regions 33 to 35. In this example the optical means for changing the light beam characteristic is several spherical lenses 44 with a center point which is located over the center of mass of each component luminous region. Here instead of lenses 44 several Fresnel lenses are likewise possible.

The window layer 2 can advantageously also be a cultivated epitaxial layer of a material which is transparent to the emitted light. Individual epitaxial layers or also the initial epitaxy material, often also called the "substrate" in the narrower sense of epitaxy process engineering, can be removed entirely or partially in known processes, for example, etched away. Likewise it is possible to join mechanically and mainly optically different material layers "seamlessly" to one another using process engineering, for example by anodic bonding or by pressing very flat surfaces onto one another.

The structures described here can also be produced very differently.

Finally, Figure 5 shows a schematic cross section through a wafer 501 with LED chips which are to be separated 505 to 507 and which have already been separated 502 - 504. The optical lenses 41 are produced by the correspondingly shaped saw blade 510 which

rotates around the axis 511 simultaneously with separation into the surface 508 of the wafer 501.

The saw blade 510 in its cross section has a thinner part 512 which runs to a point and a widening part 513 which (negatively) corresponds to the shape of the lens to be produced. The saw blade can also be shaped such that the part 512 which runs to a point is shorter so that a multiple lens structure can be made in the surface of the LED chip.

Claims

1. LED chip (1) with a radiation-emitting active region (32) with a lateral cross sectional area F_L and a radiation-transparent window layer (2) downstream of the radiation-emitting active area (32) in the emission direction, with a refractive index n_s which has a lateral cross sectional area F_c for light decoupling and which has a decoupling surface which borders a medium with a refractive index n_M,
characterized in that
the cross sectional area F_L of the radiation-emitting active area (32) is smaller than the cross sectional area F_c of the decoupling surface, the following applying

$$F_L \leq \left(n_M / n_s\right)^2 \cdot F_c$$

2. LED chip as claimed in claim 1, wherein the radiation-emitting active region (32) is defined by means of limitation of the current flow to the surface F_L of the radiation-emitting active area (32).

3. LED chip as claimed in one of claims 1 and 2, wherein the following applies to the thickness H of the window layer (2):

$$H < \left(n_s / n_M\right) \cdot \frac{1}{2} \cdot C,$$

C being the lateral cross sectional length of the window layer (2) and thus the effective reflex surface.

4. LED chip as claimed in claim 3, wherein the following applies to the thickness H of the window layer (2):

$$H = (C - D) \cdot \left(2 \cdot \left(n_M / n_s\right)\right)^{-1}$$

D being the lateral cross sectional length of the radiation-emitting active region (32).

5. LED chip as claimed in one of claims 1 to 4, wherein the light-emitting active region consists of several active component regions (33 to 35) which are located at a regular interval to one another, the following applying to the entire area F_L of the component regions:

$$\sum_i F_{Li} = F_L \leq \left(n_M / n_S\right) \cdot F_C$$

F_{Li} being the areas of the individual component regions.

6. LED chip as claimed in claim 5, wherein the following applies to the thickness H of the window layer (2):

$$H = p \cdot A$$

A being the regular interval of the individual component areas and p being a factor which can be chosen between 0.5 and 5.

7. LED chip as claimed in one of claims 1 to 6, wherein there is an optical means (41, 42, 43, 44) for concentrating the electromagnetic radiation on the window layer (2).

8. LED chip as claimed in claim 7, wherein the optical means is formed by a lens (41) with a center point which lies over the center of mass of the radiation-emitting active region (32) or by several lenses (44) with center points which lie over the center of mass of the respectively assigned active component luminous areas (33 to 35).

9. LED chip as claimed in claim 8, wherein the lenses (41, 44) are made at least partially as Fresnel lenses (42, 43) or as spherical lenses.

10. LED chip as claimed in one of claims 1 to 9, wherein the area F_L or areas F_{Li} of the radiation-emitting active regions (32, 33 to 35) is defined by limiting the luminous capacity of an active layer (3) to the area F_L or areas F_{Li} of the radiation-emitting active regions (32, 33 to 35).

11. LED chip as claimed in one of claims 1 to 9, wherein the area F_L or areas F_{Li} of the radiation-emitting active region (32, 33 to 35) is defined by an insulating layer which is made on or at one active layer (3) and which is formed from a material which is of limited translucency and/or which is at least partially opaque to the emission light of the active layer.

12. LED chip as claimed in one of claims 1 to 9, wherein the area F_L or areas F_{Li} of the radiation-emitting active regions (32, 33 to 35) is defined by an insulating layer (5) which is made on or

at one active layer (3) and between the active layer (3) and a power supply (6) and which minimizes the power supply or the current flow to or through the active layer (3) in regions (31) outside of the light-emitting area (32, 33 to 35).

13. LED chip as claimed in claim 12, wherein the insulating layer (5) consists of a nonconductive oxide layer which is applied on the side opposite the effective reflex surface (8) of the chip.

14. LED chip as claimed in one of the preceding claims, wherein a second power supply (71) is formed by the electrical contact which does not completely cover it on the effective reflex surface (8) or on the optical means (41, 42, 43, 44).

15. LED chip as claimed in one of the preceding claims, wherein the second power supply (72) is formed by an electrical contact which is located on the side of the window layer (2) facing away from the effective reflex surface (80 and which is connected to the window layer (2).

16. LED chip as claimed in one of the preceding claims, wherein the second power supply (73) is formed by an electrical contact which is connected to the active layer.

17. LED chip as claimed in one of the preceding claims, wherein the power supplies (6, 71, 72, 73, 74) and/or the insulating layer (5) are reflective to the emitted light.

18. LED chip as claimed in one of the preceding claims, wherein the reflection means for the emitted light is formed on the side of the active layer (3) which faces away from the effective reflex surface (8) in or on the window layer (2) or the active layer (3).
19. LED chip as claimed in claim 18, wherein the reflection means is a Bragg grating.

20. LED chip as claimed in one of the preceding claims, wherein the window layer (2) and/or the optical means (41, 42, 43, 44) is at least partially provided with a jacket which is transparent to the emission light.

21. LED chip as claimed in one of the preceding claims, wherein it is a light-emitting diode (LED).

22. Process for producing a lens structure on the surface of a light-emitting component, especially as claimed in one of claims 1 to 24,
wherein
the lens structure (42, 43) is shaped by means of a cutting or sawing tool or etching process from the light-emitting component (1) and into the outside surface (8) on the outside surface (8)

of the light-emitting component (1) intended for light exit and passage.

23. Process for producing a lens structure as claimed in claim 22, wherein a spherical lens (41) or a Fresnel lens (42, 43) is produced as a lens structure.

24. Process for producing a lens structure as claimed in claim 22 or 23, wherein the lens structure is produced by a sawing (510) or cutting tool and in the separation of the light-emitting components still located in the wafer array.

25. Process for producing a lens structure as claimed in claim 24, wherein the sawing (510) or the cutting tool has a narrow part (512) for separating the individual semiconductor components (502 to 507) from the wafer array (501) and a part (513) shaped according to the shape of the lens (41), for producing the lens (41).

Fig 1

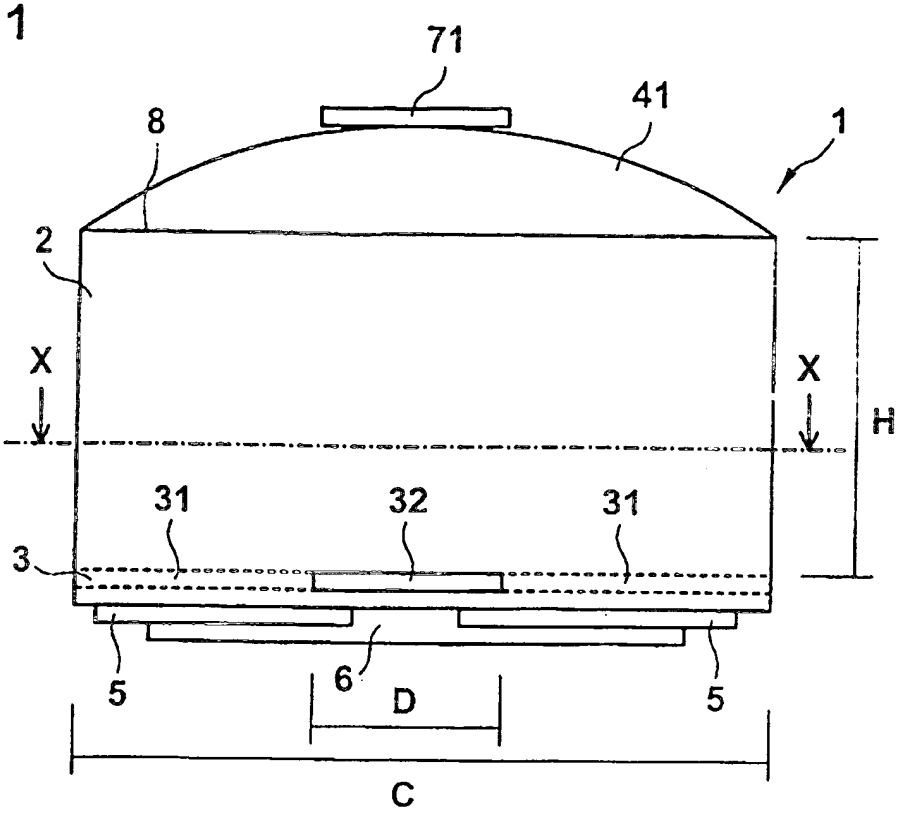


Fig 1a

X:

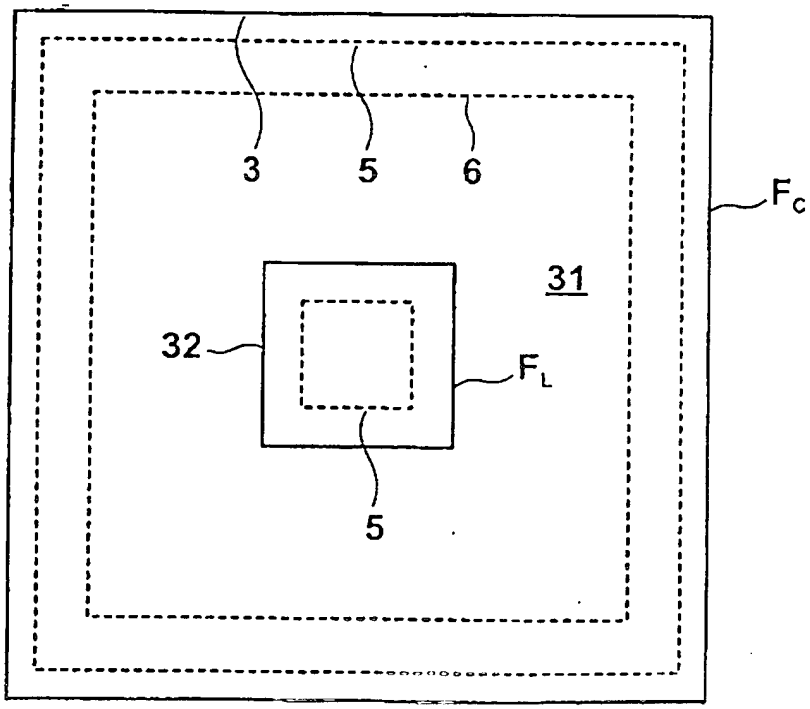


Fig 2

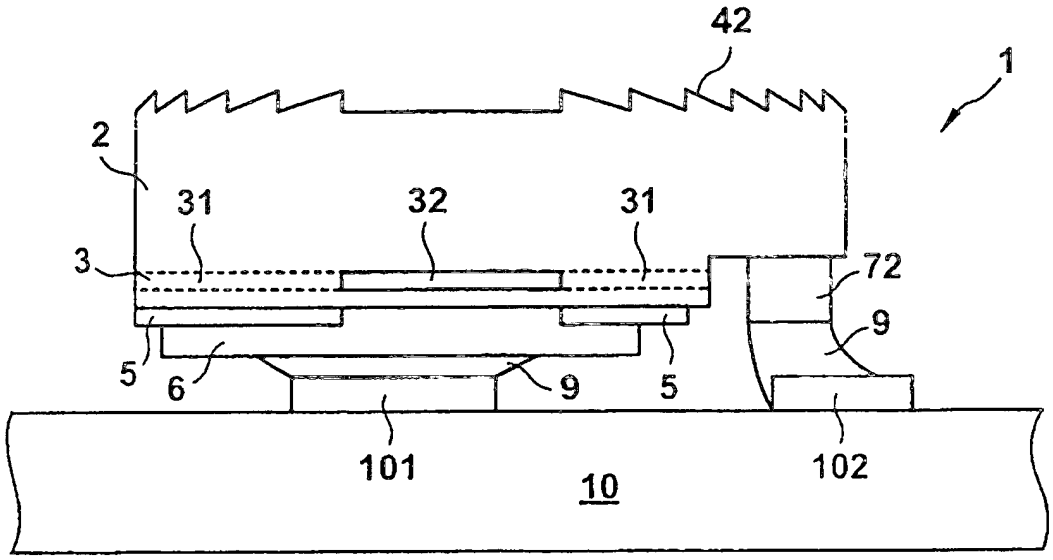


Fig 3

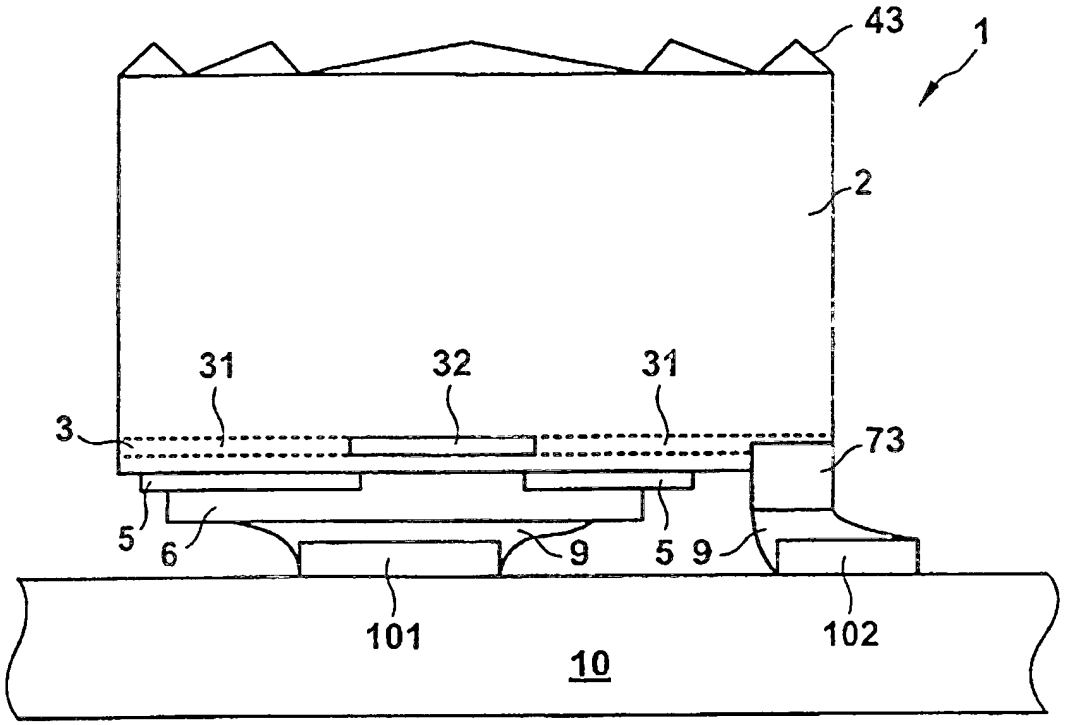

43
1
2
31
32
31
3
73
5
6
9
5
9
101
102
10

Fig 4

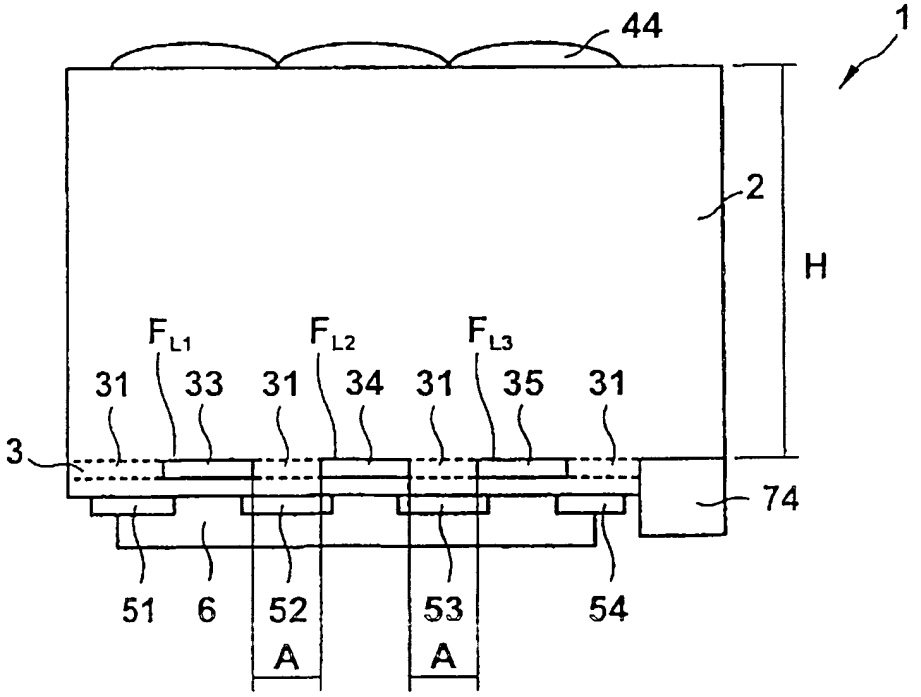
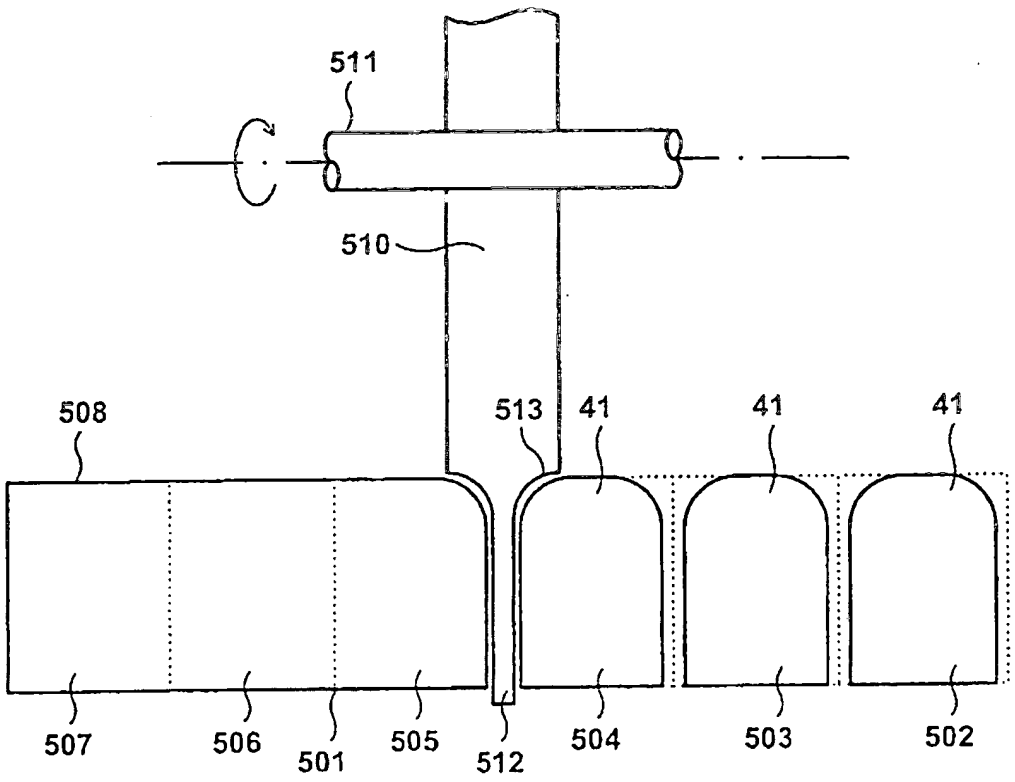

44
1
2
H
F_{L1}
F_{L2}
F_{L3}
31
33
31
34
31
35
31
3
74
51
6
52
53
54
A
A

Fig 5



(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

(19) Weltorganisation für geistiges Eigentum
Internationales Büro

(43) Internationales Veröffentlichungsdatum
25. Oktober 2001 (25.10.2001)

PCT

(10) Internationale Veröffentlichungsnummer
WO 01/80322 A3

(51) Internationale Patentklassifikation[7]: H01L 33/00, 27/15

(21) Internationales Aktenzeichen: PCT/DE01/01513

(22) Internationales Anmeldedatum:
19. April 2001 (19.04.2001)

(25) Einreichungssprache: Deutsch

(26) Veröffentlichungssprache: Deutsch

(30) Angaben zur Priorität:
100 19 665.9 19. April 2000 (19.04.2000) DE

(71) Anmelder *(für alle Bestimmungsstaaten mit Ausnahme von US)*: **OSRAM OPTO SEMICONDUCTORS GMBH & CO. OHG** [DE/DE]; Wernerwerkstrasse 2, 93049 Regensburg (DE).

(72) Erfinder; und

(75) Erfinder/Anmelder *(nur für US)*: **BOGNER, Georg** [DE/DE]; Am Sandhügel 12, 93138 Lappersdorf (DE). **KUGLER, Siegmar** [DE/DE]; Coulmierstrasse 1, 93055 Regensburg (DE). **NEUMANN, Gerald** [DE/DE]; Augustenstrasse 19, 93049 Regensburg (DE). **NIRSCHL, Ernst** [DE/DE]; Rother Weg 7a, 93173 Wenzenbach (DE). **OBERSCHMID, Raimund** [DE/DE]; Minoritenweg 7 B, 93161 Sinzing (DE). **SCHLERETH, Karl-Heinz** [DE/DE]; Akazienweg 21, 93133 Burglengenfeld (DE). **SCHOENFELD, Olaf** [DE/DE]; Kollwitz-Strasse 55, 93055 Regensburg (DE). **STATH, Norbert** [DE/DE]; Rosinusweg 11, 93049 Regensburg (DE).

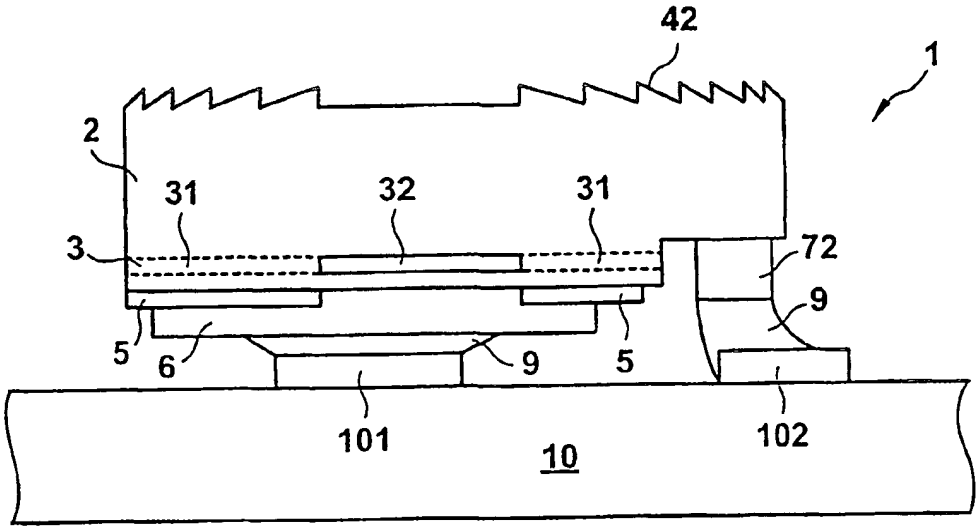
(74) Anwalt: **EPPING HERMANN & FISCHER**; Postfach 12 10 26, 80034 München (DE).

(81) Bestimmungsstaaten *(national)*: CA, CN, JP, KR, US.

[Fortsetzung auf der nächsten Seite]

(54) **Title:** HIGH-RADIANCE LED CHIP AND A METHOD FOR PRODUCING THE SAME

(54) **Bezeichnung:** LUMINESZENZDIODENCHIP UND VERFAHREN ZU DESSEN HERSTELLUNG



(57) Abstract: The invention relates to a high-radiance LED chip (1) comprising a radiation-emitting active region (32) and a window layer (2). In order to increase the radiant yield, the cross-sectional surface of the radiation-emitting active region (32) is smaller than the cross-sectional surface of the window layer (2), which is made available for disengaging the light. The invention also relates to a method for producing a lens structure on the surface of a light emitting component.

[Fortsetzung auf der nächsten Seite]

WO 01/80322 A3

(84) **Bestimmungsstaaten** *(regional)*: europäisches Patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Veröffentlicht:
— *mit internationalem Recherchenbericht*

(88) **Veröffentlichungsdatum des internationalen Recherchenberichts:** 28. März 2002

Zur Erklärung der Zweibuchstaben-Codes und der anderen Abkürzungen wird auf die Erklärungen ("Guidance Notes on Codes and Abbreviations") am Anfang jeder regulären Ausgabe der PCT-Gazette verwiesen.

(57) **Zusammenfassung:** Di Erfindung betrifft einen Lumineszenzdiodenchip (1) mit einem strahlungsemittierenden aktiven Bereichs (32), und einer Fensterschicht (2), wobei zur Steigerung der Strahlungsausbeute die Querschnittsfläche des strahlungsemittierenden aktiven Bereich (32) kleiner als die zur Lichtauskopplung zur Verfügung stehende Querschittsfläche der Fensterschicht (2) ist. Weiterhin bezieht sich die Erfindung auf ein Verfahren zur Herstellung einer Linsenstruktur auf der Oberfläche eines lichtemittierenden Bauelements.

INTERNATIONAL SEARCH REPORT

In tional Application No
PCT/DE 01/01513

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L33/00 H01L27/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 96 37000 A (SIEMENS AG) 21 November 1996 (1996-11-21) the whole document	1-3, 12-14, 17-21 7-11,15, 16

Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 243 (E-277), 8 November 1984 (1984-11-08) & JP 59 121985 A (NIPPON DENKI KK), 14 July 1984 (1984-07-14) abstract	10

Y	EP 0 977 280 A (IMEC; UNIV BRUXELLES) 2 February 2000 (2000-02-02) paragraphs '0068!,'0107!; figures 7,28	7-9,11, 15

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 October 2001	24. 10. 2001
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	**Authorized officer** van der Linden, J.E.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/DE 01/01513

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	GB 2 326 023 A (HEWLETT PACKARD CO) 9 December 1998 (1998-12-09) page 15, paragraph 3 -page 16, paragraph 1	16
X	EP 0 405 757 A (HEWLETT PACKARD CO) 2 January 1991 (1991-01-02)	1,2,5,6, 12-14, 17,18, 20,21
A	the whole document	22,24,25
X	EP 0 101 368 A (THOMSON CSF) 22 February 1984 (1984-02-22)	1-3,5-9, 14,21-23
A	the whole document	4,12
X	DE 26 33 942 A (CENTRE ELECTRON HORLOGER) 2 February 1978 (1978-02-02)	1-3, 5-10, 21-23
A	page 7, paragraph 6; figure 1	4
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 336 (E-0953), 19 July 1990 (1990-07-19) & JP 02 113524 A (HITACHI LTD;OTHERS: 01), 25 April 1990 (1990-04-25) abstract	1,2,7-9, 14,21-23
X	US 4 339 689 A (YAMANAKA H ET AL) 13 July 1982 (1982-07-13) the whole document	1-3,7-9, 12,21-23
A	WO 99 00851 A (SIEMENS AG) 7 January 1999 (1999-01-07) the whole document	1-4, 12-14, 17-21
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 313 (E-448), 24 October 1986 (1986-10-24) & JP 61 125092 A (NEC CORP), 12 June 1986 (1986-06-12) abstract	1-4, 10-14, 17,18,21
A	US 5 264 715 A (GUENTER J ET AL) 23 November 1993 (1993-11-23) column 8, line 15 -column 10, line 4	1-4, 10-12, 18,19
A	US 5 705 834 A (ROGOWSKI R ET AL) 6 January 1998 (1998-01-06) the whole document	1-4,21

-/--

2

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/DE 01/01513

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 02, 28 February 1997 (1997-02-28) -& JP 08 255933 A (OMRON CORP), 1 October 1996 (1996-10-01) the whole document	1,2,7-9, 11,14, 21-23
A	EP 0 562 880 A (NIPPON ELECTRIC CO) 29 September 1993 (1993-09-29) column 8, line 10-57	22,24

2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DE 01/01513

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See supplemental sheet FURTHER INFORMATION PCT/ISA/210

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

The International Searching Authority found that this International Application contains several inventions or groups of inventions. as follows:

1. Claims nos: 1-6. 10-21

   High-radiance LED chip comprising a radiation-emitting active region of specific lateral dimensions in comparison to the disengaging surface.

2. Claims nos: 7-9. 22-25

   High-radiance LED chip comprising a lens and a method for producing the same.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ional Application No
PCT/DE 01/01513

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 9637000	A	21-11-1996	WO	9637000 A1	21-11-1996
JP 59121985	A	14-07-1984	NONE		
EP 0977280	A	02-02-2000	EP	0977063 A1	02-02-2000
			EP	0977280 A2	02-02-2000
			EP	0977277 A1	02-02-2000
			EP	0977064 A1	02-02-2000
			JP	2000098180 A	07-04-2000
			JP	2000106454 A	11-04-2000
GB 2326023	A	09-12-1998	US	6229160 B1	08-05-2001
			DE	19807758 A1	10-12-1998
			JP	10341035 A	22-12-1998
			US	2001000209 A1	12-04-2001
			US	2001000410 A1	26-04-2001
EP 0405757	A	02-01-1991	EP	0405757 A2	02-01-1991
			JP	3035568 A	15-02-1991
			US	5087949 A	11-02-1992
EP 0101368	A	22-02-1984	FR	2531814 A1	17-02-1984
			EP	0101368 A2	22-02-1984
			JP	59051580 A	26-03-1984
DE 2633942	A	02-02-1978	DE	2633942 A1	02-02-1978
JP 02113524	A	25-04-1990	NONE		
US 4339689	A	13-07-1982	JP	55102282 A	05-08-1980
			CA	1147050 A1	24-05-1983
			GB	2043340 A ,B	01-10-1980
WO 9900851	A	07-01-1999	DE	19727233 A1	07-01-1999
			CN	1261462 T	26-07-2000
			WO	9900851 A1	07-01-1999
			EP	0996984 A1	03-05-2000
JP 61125092	A	12-06-1986	NONE		
US 5264715	A	23-11-1993	NONE		
US 5705834	A	06-01-1998	NONE		
JP 08255933	A	01-10-1996	NONE		
EP 0562880	A	29-09-1993	DE	69312360 D1	28-08-1997
			DE	69312360 T2	20-11-1997
			EP	0562880 A1	29-09-1993
			JP	6013650 A	21-01-1994
			US	5349211 A	20-09-1994

INTERNATIONALER RECHERCHENBERICHT

Int. Internales Aktenzeichen
PCT/DE 01/01513

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 7 H01L33/00 H01L27/15

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 7 H01L

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)
EPO-Internal, PAJ

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
X	WO 96 37000 A (SIEMENS AG) 21. November 1996 (1996-11-21)	1-3, 12-14, 17-21
Y	das ganze Dokument	7-11,15, 16

Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 243 (E-277), 8. November 1984 (1984-11-08) & JP 59 121985 A (NIPPON DENKI KK), 14. Juli 1984 (1984-07-14) Zusammenfassung	10

Y	EP 0 977 280 A (IMEC; UNIV BRUXELLES) 2. Februar 2000 (2000-02-02) Absätze '0068!,'0107!; Abbildungen 7,28	7-9,11, 15

	-/--	

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

[X] Siehe Anhang Patentfamilie

° Besondere Kategorien von angegebenen Veröffentlichungen
"A" Veröffentlichung, die den allgemeinen Stand der Technik definiert, aber nicht als besonders bedeutsam anzusehen ist
"E" älteres Dokument, das jedoch erst am oder nach dem internationalen Anmeldedatum veröffentlicht worden ist
"L" Veröffentlichung, die geeignet ist, einen Prioritätsanspruch zweifelhaft erscheinen zu lassen, oder durch die das Veröffentlichungsdatum einer anderen im Recherchenbericht genannten Veröffentlichung belegt werden soll oder die aus einem anderen besonderen Grund angegeben ist (wie ausgeführt)
"O" Veröffentlichung, die sich auf eine mündliche Offenbarung, eine Benutzung, eine Ausstellung oder andere Maßnahmen bezieht
"P" Veröffentlichung, die vor dem internationalen Anmeldedatum, aber nach dem beanspruchten Prioritätsdatum veröffentlicht worden ist
"T" Spätere Veröffentlichung, die nach dem internationalen Anmeldedatum oder dem Prioritätsdatum veröffentlicht worden ist und mit der Anmeldung nicht kollidiert, sondern nur zum Verständnis des der Erfindung zugrundeliegenden Prinzips oder der ihr zugrundeliegenden Theorie angegeben ist
"X" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann allein aufgrund dieser Veröffentlichung nicht als neu oder auf erfinderischer Tätigkeit beruhend betrachtet werden
"Y" Veröffentlichung von besonderer Bedeutung; die beanspruchte Erfindung kann nicht als auf erfinderischer Tätigkeit beruhend betrachtet werden, wenn die Veröffentlichung mit einer oder mehreren anderen Veröffentlichungen dieser Kategorie in Verbindung gebracht wird und diese Verbindung für einen Fachmann naheliegend ist
"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
8. Oktober 2001	24 10 2001

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	van der Linden, J.E.

2

Formblatt PCT/ISA/210 (Blatt 2) (Juli 1992)

INTERNATIONALER RECHERCHENBERICHT

Int. Amtliches Aktenzeichen
PCT/DE 01/01513

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y	GB 2 326 023 A (HEWLETT PACKARD CO) 9. Dezember 1998 (1998-12-09) Seite 15, Absatz 3 -Seite 16, Absatz 1	16
X	EP 0 405 757 A (HEWLETT PACKARD CO) 2. Januar 1991 (1991-01-02)	1,2,5,6, 12-14, 17,18, 20,21
A	das ganze Dokument	22,24,25
X	EP 0 101 368 A (THOMSON CSF) 22. Februar 1984 (1984-02-22)	1-3,5-9, 14,21-23
A	das ganze Dokument	4,12
X	DE 26 33 942 A (CENTRE ELECTRON HORLOGER) 2. Februar 1978 (1978-02-02)	1-3, 5-10, 21-23
A	Seite 7, Absatz 6; Abbildung 1	4
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 336 (E-0953), 19. Juli 1990 (1990-07-19) & JP 02 113524 A (HITACHI LTD;OTHERS: 01), 25. April 1990 (1990-04-25) Zusammenfassung	1,2,7-9, 14,21-23
X	US 4 339 689 A (YAMANAKA H ET AL) 13. Juli 1982 (1982-07-13) das ganze Dokument	1-3,7-9, 12,21-23
A	WO 99 00851 A (SIEMENS AG) 7. Januar 1999 (1999-01-07) das ganze Dokument	1-4, 12-14, 17-21
A	PATENT ABSTRACTS OF JAPAN vol. 010, no. 313 (E-448), 24. Oktober 1986 (1986-10-24) & JP 61 125092 A (NEC CORP), 12. Juni 1986 (1986-06-12) Zusammenfassung	1-4, 10-14, 17,18,21
A	US 5 264 715 A (GUENTER J ET AL) 23. November 1993 (1993-11-23) Spalte 8, Zeile 15 -Spalte 10, Zeile 4	1-4, 10-12, 18,19
A	US 5 705 834 A (ROGOWSKI R ET AL) 6. Januar 1998 (1998-01-06) das ganze Dokument	1-4,21

-/—

2

INTERNATIONALER RECHERCHENBERICHT

In	denales Aktenzeichen
	PCT/DE 01/01513

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie°	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 02, 28. Februar 1997 (1997-02-28) -& JP 08 255933 A (OMRON CORP), 1. Oktober 1996 (1996-10-01) das ganze Dokument	1,2,7-9, 11,14, 21-23
A	EP 0 562 880 A (NIPPON ELECTRIC CO) 29. September 1993 (1993-09-29) Spalte 8, Zeile 10-57	22,24

INTERNATIONALER RECHERCHENBERICHT

amtliches Aktenzeichen
PCT/DE 01/01513

Feld I Bemerkungen zu den Ansprüchen, die sich als nicht recherchierbar erwiesen haben (Fortsetzung von Punkt 2 auf Blatt 1)

Gemäß Artikel 17(2)a) wurde aus folgenden Gründen für bestimmte Ansprüche kein Recherchenbericht erstellt:

1. ☐ Ansprüche Nr.
weil sie sich auf Gegenstände beziehen, zu deren Recherche die Behörde nicht verpflichtet ist, nämlich

2. ☐ Ansprüche Nr.
weil sie sich auf Teile der internationalen Anmeldung beziehen, die den vorgeschriebenen Anforderungen so wenig entsprechen, daß eine sinnvolle internationale Recherche nicht durchgeführt werden kann, nämlich

3. ☐ Ansprüche Nr.
weil es sich dabei um abhängige Ansprüche handelt, die nicht entsprechend Satz 2 und 3 der Regel 6.4 a) abgefaßt sind.

Feld II Bemerkungen bei mangelnder Einheitlichkeit der Erfindung (Fortsetzung von Punkt 3 auf Blatt 1)

Die internationale Recherchenbehörde hat festgestellt, daß diese internationale Anmeldung mehrere Erfindungen enthält:

siehe Zusatzblatt

1. ☒ Da der Anmelder alle erforderlichen zusätzlichen Recherchengebühren rechtzeitig entrichtet hat, erstreckt sich dieser internationale Recherchenbericht auf alle recherchierbaren Ansprüche.

2. ☐ Da für alle recherchierbaren Ansprüche die Recherche ohne einen Arbeitsaufwand durchgeführt werden konnte, der eine zusätzliche Recherchengebühr gerechtfertigt hätte, hat die Behörde nicht zur Zahlung einer solchen Gebühr aufgefordert.

3. ☐ Da der Anmelder nur einige der erforderlichen zusätzlichen Recherchengebühren rechtzeitig entrichtet hat, erstreckt sich dieser internationale Recherchenbericht nur auf die Ansprüche, für die Gebühren entrichtet worden sind, nämlich auf die Ansprüche Nr.

4. ☐ Der Anmelder hat die erforderlichen zusätzlichen Recherchengebühren nicht rechtzeitig entrichtet. Der internationale Recherchenbericht beschränkt sich daher auf die in den Ansprüchen zuerst erwähnte Erfindung; diese ist in folgenden Ansprüchen erfaßt:

Bemerkungen hinsichtlich eines Widerspruchs

☐ Die zusätzlichen Gebühren wurden vom Anmelder unter Widerspruch gezahlt.

☒ Die Zahlung zusätzlicher Recherchengebühren erfolgte ohne Widerspruch.

WEITERE ANGABEN PCT/ISA/ 210

Die internationale Recherchenbehörde hat festgestellt, daß diese internationale Anmeldung mehrere (Gruppen von) Erfindungen enthält, nämlich:

1. Ansprüche: 1-6,10-21

   Lumineszenzdiodenchip mit einem strahlungsemittierenden aktiven Bereich von bestimmter lateraler Abmessung im Vergleich mit der Auskoppelfläche

2. Ansprüche: 7-9,22-25

   Lumineszenzdiodenchip mit einer Linse und Verfahren zur Herstellung

INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichungen, die zur selben Patentfamilie gehören

nt... ...enales Aktenzeichen
PCT/DE 01/01513

Im Recherchenbericht angeführtes Patentdokument		Datum der Veröffentlichung	Mitglied(er) der Patentfamilie		Datum der Veröffentlichung
WO 9637000	A	21-11-1996	WO	9637000 A1	21-11-1996
JP 59121985	A	14-07-1984	KEINE		
EP 0977280	A	02-02-2000	EP	0977063 A1	02-02-2000
			EP	0977280 A2	02-02-2000
			EP	0977277 A1	02-02-2000
			EP	0977064 A1	02-02-2000
			JP	2000098180 A	07-04-2000
			JP	2000106454 A	11-04-2000
GB 2326023	A	09-12-1998	US	6229160 B1	08-05-2001
			DE	19807758 A1	10-12-1998
			JP	10341035 A	22-12-1998
			US	2001000209 A1	12-04-2001
			US	2001000410 A1	26-04-2001
EP 0405757	A	02-01-1991	EP	0405757 A2	02-01-1991
			JP	3035568 A	15-02-1991
			US	5087949 A	11-02-1992
EP 0101368	A	22-02-1984	FR	2531814 A1	17-02-1984
			EP	0101368 A2	22-02-1984
			JP	59051580 A	26-03-1984
DE 2633942	A	02-02-1978	DE	2633942 A1	02-02-1978
JP 02113524	A	25-04-1990	KEINE		
US 4339689	A	13-07-1982	JP	55102282 A	05-08-1980
			CA	1147050 A1	24-05-1983
			GB	2043340 A ,B	01-10-1980
WO 9900851	A	07-01-1999	DE	19727233 A1	07-01-1999
			CN	1261462 T	26-07-2000
			WO	9900851 A1	07-01-1999
			EP	0996984 A1	03-05-2000
JP 61125092	A	12-06-1986	KEINE		
US 5264715	A	23-11-1993	KEINE		
US 5705834	A	06-01-1998	KEINE		
JP 08255933	A	01-10-1996	KEINE		
EP 0562880	A	29-09-1993	DE	69312360 D1	28-08-1997
			DE	69312360 T2	20-11-1997
			EP	0562880 A1	29-09-1993
			JP	6013650 A	21-01-1994
			US	5349211 A	20-09-1994